

DOCKET NO. PEARCE 27

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Charles W. Pearce

Serial No.: 09/755,828

Filed: January 4, 2001

For: METHOD FOR MANUFACTURING A Laterally Diffused  
Metal Oxide Semiconductor Device

Group No.: 2893

Examiner: Jack S.J. Chen

Confirmation No.: 5397

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

I hereby certify that this correspondence is being electronically filed with  
United States Patent and trademark Office on:

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Elizabeth Schumacher

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### **ELECTION OF CLAIMS WITH TRAVERSE**

In response to the Official Action of February 5, 2009, Applicant hereby elects, with traverse, Claims 1-3 and 6-10, comprising Group I.

The Applicant submits that the restriction requirement is improper for a number of reasons. First, the restriction is improper since a search and examination has already been performed on the claims. As stated in section 803 of the MPEP: "If the search and examination of an entire application can be made without serious burden, the examiner *must* examine it on the merits, even though it includes claims to independent or distinct inventions." (Emphasis added.) Since a search and examination has already been performed with respect to the numerous Office Actions prior to the instant one, the present pending claims do not present a serious search and examination burden.

Second, the Applicant submits that the Examiner's reasons for issuing the restriction requirement are faulty, and lacking support. Namely, the Examiner indicates that "[t]he subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination I has separate utility such as memory device. See MPEP §806.05(d)." See, page 2 paragraph 2 of the Restriction Requirement dated February 5, 2009. It should be noted that the three items listed above are inclusive, as opposed to exclusive. Accordingly, all must be met before the subcombinations can be considered distinct. Nevertheless, the Examiner only attempts to establish the third of the three requirements, and entirely fails to address the first two—namely, that they do not overlap in scope and are not obvious variants. As the Examiner is well aware, independent Claim 11 includes the exact same language contained within independent Claim 1, but adds an interlevel dielectric layer

located over the LDMOS, as well as interconnects therein for electrical connection thereto. Accordingly, independent Claims 1 and 11 clearly overlap in scope, even with the addition of these two items.

Third, the Applicant submits that a restriction is no more warranted now than it was warranted in any of the previous Examiner's Actions. For example, from the initial filing of the instant case, independent Claims 1 and 11 mirrored each other but for the addition of the interlevel dielectric layer located over the LDMOS, as well as the interconnects therein for electrical connection thereto, which is further included within independent Claim 11. Nowhere in the previous half dozen Examiner's Actions did the Examiner indicate that a restriction was required with regard to independent Claims 1 and 11. Why now is a restriction relevant, when Claims 1 and 11 track each other in much the same way they did as originally filed? Simply put, a restriction requirement was not warranted then, and is not warranted now.

For the foregoing reasons, the Applicant respectfully requests that the restriction requirement be withdrawn. Group I (Claims 1-3 and 6-10), Group II (Claims 11-13 and 16-20) are listed below.